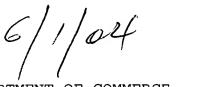
UNITED STATES DEPARTMENT OF COMMERCE

Alexandria, VA 22313-1450





PATENT AND TRADEMARK OFFICE

App Serial No: 09/825,377) Confirmation: 1648
Applicant(s): Yi Hů Zhiping Sun	RECEIVED
Filing Date: 04/02/2001) JUN 0 4 2004
TC/A.U.: 2655 Docket: KELLY-4 EXAMINER: Smits, Talivaldis Ivars Title: CODEC WITH VECTOR PROCESSOR-BASED	Technology Center 2600
ACCELERATOR CORE) Ph: (703)306-3011) Fax:(703)872-9314
Commissioner for Patents P.O. Box 1450	

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 CFR section 1.97, the Applicant submits the following information, accompanied by a best copy of the cited documents. Form PTO 1449 is attached. A detailed discussion will follow.

By submitting these materials, the applicant does not concede that all are prior art. They do not know when some of the competitive devices were first made public.

Introduction:

The following disclosure is being transmitted in the form provided to the attorney for applicant.

Some of the references appear to be relevant to, or useful in, evaluating the present patent application. For the purpose of completeness and accuracy, the reference is enclosed.

Patents:

The following reference was cited by the overseas attorney for the inventor on May 13, 2004, and received on September 1, 2000:

- U.S. Patent No. 5,987,556 to Nakagawa entitled "DATA PROCESSING DEVICE HAVING ACCELLERATOR FOR DIGITAL SIGNAL PROCESSING". A data processor structure is disclosed..
- U.S. Patent No. 5,727,123 to McDonough entitled "BLOCK NORMALIZATION PROCESSOR". A vocoder implementation method is disclosed.

Other:

Paper "HALF-RATE GSM VOCODER IMPLEMENTATION ON A DUAL MAC DIGITAL SIGNAL PROCESSOR", 1997 IEEE publication

Paper "HIERARCHIAL VHDL LIBRARIES FOR DSP ASIC DESIGN" 1997 IEEE publication

Abstract from European Patent Application EP 2 248 252 A3, showing a March 31, 2004 publication date.

RECEIPT WITHOUT FEE DUE

N	<u>/a</u>		Certification
Atto	orney for Ap	plica	ant Certifies that:
		(0)	This disclosure statement is being filed with
the	patent appl	icat	ion.
	XXX	(1)	That each item of information contained in
the	information	n dis	closure statement was cited in a

communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the statement, or

That no item of information contained XXX (2) in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the person signing the certification after making reasonable inquiry, was known to any individual designated in # 1.56(c) more than three months prior to the filing of the statement. (Cited in related U.S. Application)

For the foregoing reasons, the Applicants submits that these references neither disclose nor suggest the claimed invention.

Dated:

May 28, 2004

Respectfully submitted:

Curt Harrington

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"EXPRESS MAIL" MAILING LABEL NUMBER: EV 329 192 781 US

DATE OF DEPOSIT: May 28, 2004
I HEREBY CERTIFY THAT THIS PAPER OR FEE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED ABOVE AND IS

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Curtis L. Harrington, Reg. No. 31,456

PEO-1449 Page 1/1 09/825,377 KELLY-4 MAY 2 8 704 INFORMATION Yi Hu & Zhiping Sun ITATION CODEC WITH VECTOR PROCESSOR-Group Art U:2655 BASED ACCELLERATOR CORE U.S. Patent Documents Exmr | Doc. Number Sb | FD Date Name 5 9 8 7 5 5 6 11/1999 Nakagawa Prev 7 2 7 3 3/1998 McDonough et al RECEIVED JUN 0 4 2004 Technology Center 2600 FOREIGN PATENT DOCUMENTS 2 4 8 2 5 2 3/31/04 Sun & Hi 1 ΕP Copy of European Search Report for EP 01 11 3717 Paper "HALF-RATE GSM VOCODER IMPLEMENTATION ON A DUAL MAC DIGITAL SIGNAL PROCESSOR", 1997 IEEE publicaton Paper "HIERARCHIAL VHDL LIBRARIES FOR DSP ASIC DESIGN" 1997 IEEE publication